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Research Article

Switched-Capacitor Enhanced Circuits for Voltage-Boosting DC-DC Converters: Principles and Applications

Yuanqing Pan*, Dong Lv, Chuan Lu, Jiankan Lu

Suzhou Power Supply Company State Grid Jiangsu Electric Power Co., Ltd. Suzhou, China

Abstract

With rapid advancement of DC-DC converter, the non-isolated dc-dc converters has caught much attention from academia and industry, owing to its advantages including low cost and compacted structure. Especially, the non-isolated dc-dc converters have taken the dominant position in topology design of power source. This paper introduces the concept of output section evolution in non-isolated dc-dc converters, with the aim of integrating high ratio voltage boosting capacity. To achieve this, a series of novel output enhanced circuits are proposed and discussed in detail. These circuits are structured using capacitors and diodes, making them applicable to various positive output dc-dc converters. Notably, the derived topologies in this paper eliminate the need for additional power switches and transformers. The effectiveness of the proposed approach is demonstrated through application cases based on both the classical boost converter and the developed voltage-lift SEPIC converters. These cases showcase the practical application and benefits of the proposed method. By following the topology construction method outlined in the paper, engineers can gain valuable insights and guidelines for designing circuits in the field of power electronics. Theoretical analysis has been verified in experimental prototype and the provided resources also serve as an educational tool for those studying power electronics engineering.

Keywords

DC-DC Converters, Switched-Capacitor, Topology, Voltage Lift Technique, Voltage Ratio

1. Introduction

The advanced topology theories of dc-dc converters have been extensively studied over the past thirty years. These theories have been applied to construct advanced dc-dc topologies that offer high performance for a range of industrial applications [1-3]. In today's rapidly evolving technological landscape, there is a growing demand for voltage boosting dc-dc converters in sectors. In certain cases, techniques like cascade connection and the utilization of high-frequency transformers have been employed to achieve these high voltage ratio [4, 5]. However, cascade connection has limitations in terms of efficiency and complexity, as it requires multiple switches and intricate control schemes. On the other hand, high-frequency transformers utilization poses challenges due to magnetic components and the need for low switching frequencies.

To date, deeply exploration of ion-isolated dc-dc topologies

*Corresponding author: tengbaichuan@sjtu.edu.cn (Yuanqing Pan)

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enhancement. These techniques include hybrid SL/SC, voltage lift (VL) switched-capacitor (SC), switched-inductor (SL) schemes. The SC techniques [9-13] offer the advantage of eliminating the need for inductors, resulting in smaller size and higher power density. However, SC-type converters require more power switches compared to magnetic-based converters. Transformer-less hybrid converter cells were proposed for voltage-boosting dc-dc converters based on classical converters [14, 15]. These circuits can achieve high voltage ratio with single power switch, but they also involve an increase in the number of passive components. Combining the classical prototypes with the aforementioned methods could be a viable solution for promoting the applications of transformer-less double-output converters.

In contrast to traditional methods that focus on improving output performance through external factors, this paper takes a different approach by targeting the "output section" concept of dc-dc topologies themselves. By exploring and enhancing the output section, the paper aims to directly improve the output performance of dc-dc converters. This novel perspective provides a unique and innovative approach to achieving higher voltage ratios and optimizing the overall performance of dc-dc topologies.

It is observed that the output capacitor, C_o, is a common component in various topologies. The pump circuit consists of switches, diodes, and passive components, participates in the operation of all dc-dc converters. Consequently, a generalized configuration of the enhanced converter can be observed in Figure 1. Typically, the output section does not contain any components and directly delivers energy from C_o to the load, R, in each cycle. The voltage ratios of each section are denoted as M_p and M_o, respectively. As a result, the overall voltage ratio could be determined by:

$$M = \frac{V_o}{V_{in}} = M_p M_o \tag{1}$$

An example of such a dc-dc converter illustrated in Figure 2 [6], the pump section comprises components S, D_o, L, L_1 and C_s. The value of M_p in this case is equal to $D/(1\text{-}D)$. That is to say, the output section has no components, and M_o is equal to *1*. Hence, the voltage ratio of the entire SEPIC converter, as depicted in Figure 2, can be calculated by multiplying M_p and M_o together.

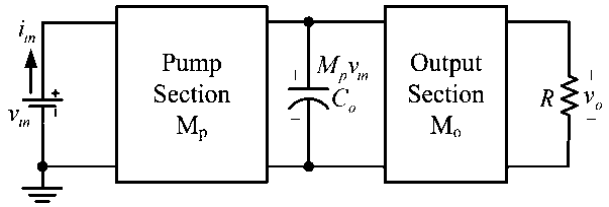

Figure 1. *General configuration of a positive output dc-dc converter.*

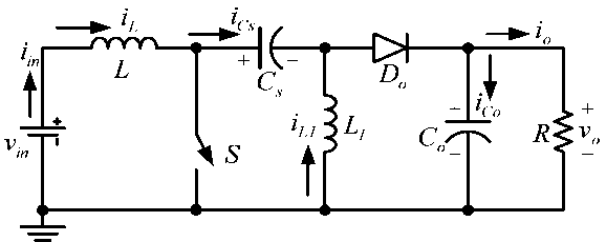

Figure 2. *Topology of the SEPIC converter.*

By maintaining the relative positioning of each component in a given converter and introducing additional components into the output section, we can achieve an enhanced output section with higher voltage ratios. These new topologies retain the fundamental advantages of the converter while significantly increasing the voltage ratio of the overall circuit, as stated in equation (1).

To address the challenges of complex control and cost associated with multiple power switches and transformers, this paper proposes the adoption of the voltage lift (*VL*) technique to evolve the output section. A series of innovative output enhanced circuits are introduced in the output section. These circuits share the common power switch with the pump section. With the improved output section, the newly proposed dc-dc converter is capable of higher voltage ratios compared to traditional ones.

We can achieve an improvement in the voltage ratio of the output section by maintaining the relative position of each component and introducing several new components. These new topologies retain the fundamental advantages of the converter and result in a significant increase in the overall circuit's voltage ratio, as expressed by equation (1). This paper introduces the voltage lift (VL) technique for implementing the enhancement of the output section. The output section is augmented with a series of innovative circuits, while sharing the same power switch as the pump section. With this improvement of the output section, the newly derived dc-dc converters offer higher voltage ratios compared to conventional ones.

2. SC Output Enhanced Circuits

The output circuit can be developed by implementing the *VL*. To construct a enhanced circuit (*EC*), diodes and capacitors (D_1-C_1-D_2-C_2) are used, as depicted in Figure 3.

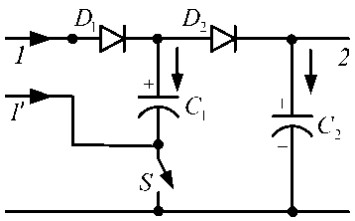

Figure 3. *Topology of the SEPIC converter.*

With assumption that the power is transmitted from node *1* to node *2*, the voltage across C_2 (V_{C2}) will be twice the voltage across capacitor C_1 (V_{C2}). This demonstrates the effectiveness of the V_L technique in enhancing the voltage ratios of dc-dc converters. Consequently, series-connected novel circuits are obtained in the output section. For convenience, they are named as the double *EC* and triple EC circuits. Generalized circuit are depicted in Figure 6 for easy reference.

2.1. Double EC

The basic voltage lift (VL) cell in the form of a double EC is depicted in Figure 4. During *S* is turned on, D_{o1} is activated while D_o and D_{o2} remain inactive. Conversely, when *S* is switched off, D_{o1} is deactivated and both D_o and D_{o2} are activated. During the turned-on phase, the voltage across C_{o1} is charged to V_{Co}. On the other hand, during the turned-off phase, V_1 becomes equal to V_{Co}. Furthermore, the output voltage V_{Co2} is determined by the sum of V_1+V_{Co1}. Due to the unique characteristics of C_{o1}, it has the ability to elevate V_{Co2} by V_{Co2}. Mathematically, this can be expressed as equation (2).

$$V_{Co2} = 2V_{Co} \tag{2}$$

It is evident from (2) that the voltage ratio of the output section M_o, could be raised from 1 to 2.

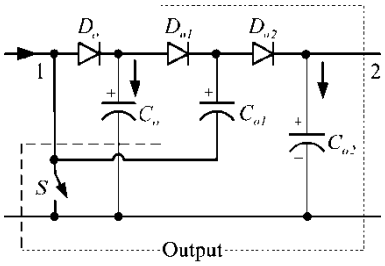

Figure 4. *Double EC studied in this paper.*

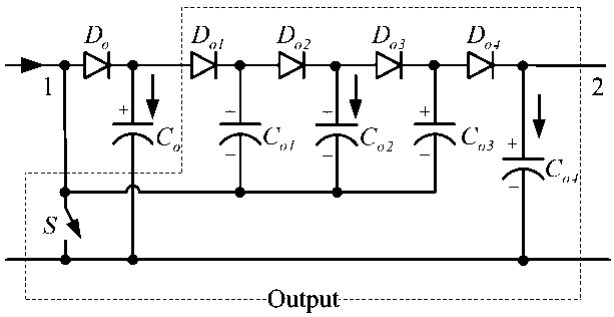

Figure 5. *Triple EC studied in this paper.*

2.2. Triple EC

The topology of triple EC is obtained by incorporating additional components (D_{o3}-C_{o3}-D_{o4}-C_{o4}) into the double EC setup. It is composed by two fundamental VL cells, as illustrated in Figure 5. Similar to the double EC, when switch *S* is turned on, D_{o1} is activated while D_o and D_{o2} remain inactive. On the other hand, when *S* is switched off, D_{o1} is deactivated and both D_o and D_{o2} are activated. During the turned-on phase, the voltage across C_{o1} is charged to V_{Co}. Similarly, during the turned-off phase, node 1's potential, V_1, becomes equal to V_{Co}. The output voltage V_{Co2} depends on the sum of V_1 and V_{Co1}. As C_{o1} possesses the capability to elevate V_{Co2} by V_{Co}, we can express this relationship using equation (3).

$$V_{Co4} = 3V_{Co} \tag{3}$$

It is evident from equation (3) that the voltage ratio of the output section M_o, could be raised from 1 to 3.

2.3. Multiple EC

It is indeed possible to create multiple voltage lift (VL) cells by replicating the components (L_2 -S_1-D_2-C_2). Given n VL cells, the generalized VL cell configuration is depicted in Figure 6. An important advantage of this setup is that all the circuits share common power switch, S. This simplifies the control system and saves costs. Each circuit in this configuration consists of one switch, *2n* capacitors, and *2n* diodes. It is important to note that all the capacitors are appropriately sized. Building upon the earlier analysis and calculations, we have derived the following general formulas that apply to all VL cells:

$$V_{Co(2n)} = (n+1)V_{Co} \tag{4}$$

Indeed, the voltage ratios are equal to *(n+1)*. This indicates that the improvement of the output circuit could be accomplished.

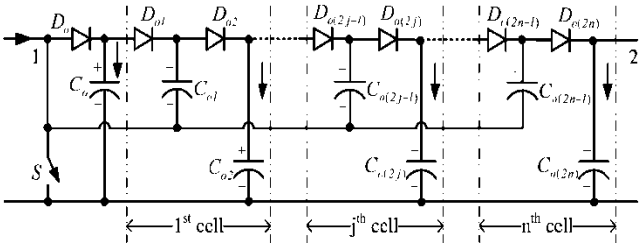

Figure 6. *Multiple EC studied in this paper.*

3. Applications to the Boost Converter

As two conversion paths share a boost converter circuit which is considered to be the common source section, we can utilize the voltage lift technique to construct corresponding enhanced circuits. A family of novel circuits are

applied to the source section, enabling them to transfer a significantly higher amount of energy to capacitors C_{s+} and C_{s-} in each cycle. As a result, the voltages V_{Cs+} and V_{Cs-} increase step-by-step along a geometric progression. For convenience, we refer to these circuits as *boost*[1], *boost*[2] and *boost*[M] enhanced circuits, respectively.

In Figure 7, the typical boost converter consists of the components D_o, L and S. In this configuration, both L and S are located in the boosting section. This arrangement allows for the use of a single power switch. However, in the proposed circuits, the L and S remain the same positions. This means that the double-EC-based boost converter requires only one power switch as well. By combining the boosting section with the double EC, a novel type of dc-dc converter is formed, as depicted in Figure 8.

Using (1) and (2), the voltage ratio of the double-EC -based enhanced boost converter could be obtained [16].

$$M = \frac{V_{Co2}}{V_{in}} = \frac{1}{1-D} \times 2 = \frac{2}{1-D} \tag{5}$$

Similar to the double-EC-based boost converter, a new type of triple-EC-based boost converter can also be proposed. This configuration is shown in Figure 9. Therefore, the voltage ratio of the new type of triple-EC-based boost converter could be obtained by

$$M = \frac{V_{Co4}}{V_{in}} = \frac{1}{1-D} \times 3 = \frac{3}{1-D} \tag{6}$$

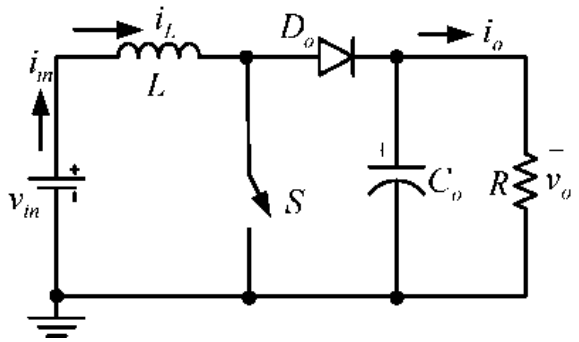

Figure 7. *The typical boost converters.*

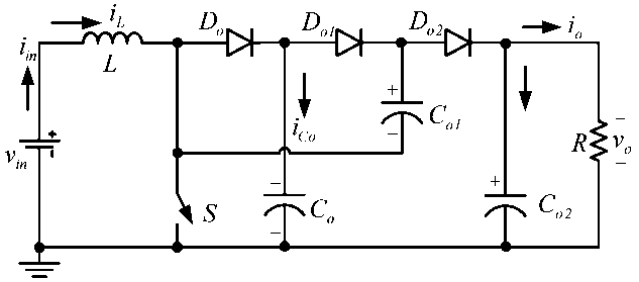

Figure 8. *The new type double EC based boost converter.*

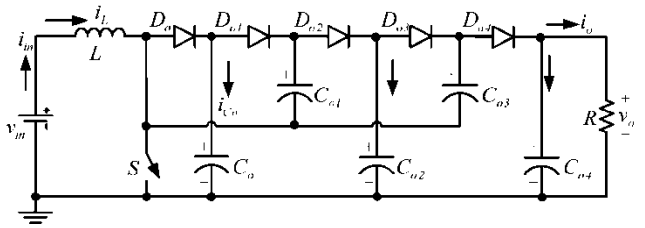

Figure 9. *The new type of triple-EC-based boost converter.*

4. Applications to the VL-Type Sepic Converters

The VL-type SEPIC converters [7, 8] are constructed with series-connected innovative voltage-boosting dc-dc converters compared to classical SEPIC converters. These converters can be classified into different categories determined by the number of VL cells, including the self-lift circuit, re-lift circuit, triple-lift circuit, and multiple circuits.

Figure 10 illustrates the VL-type SEPIC converters self-lift circuit. In this circuit, the pump section consists of components such as L, S, C_s, L_1, C_1, D_1 and D_o. Specifically, the combination of L_1-C_1-D_1 is referred to as a VL cell. The voltage ratio is obtained by:

$$M_{p-self} = \frac{1}{1-D} \tag{7}$$

In the combined pump and output section, there is no overlap, necessitating the use of two separate active power switches. However, upon further examination of the circuit's operating principles, it is found that the switching actions of D_1 are identical to those of S. As a result, the S in the output section is replaced with a passive switch D_1. This modification eliminates the need for an additional power switch, resulting in a topology that only requires a single power switch. By embedding the proposed double EC into the pump section, the resulting new dc-dc topology is shown in Figure 11. Therefore, based on equation (1) and (2), the voltage ratio is obtained by:

$$M = \frac{V_{Co2}}{V_{in}} = M_{p-self} M_o = \frac{1}{1-D} \times 2 = \frac{2}{1-D} \tag{8}$$

Similar with the self-lift circuit, it is easy and intuitive to develop the double EC based triple-lift circuit of VL-type SEPIC converters, as shown in Figure 12. In this configuration, the corresponding boosting section of the triple-lift circuit comprises (L_1-C_1-D_1, L_1-C_2-D_2-D_3, and L_3-C_3-D_4).

$$M_{p-triple} = \frac{3}{1-D} \tag{9}$$

Obviously, operation principles of D_1, D_2 and D_4 are iden-

tical to that of *S* in the output section, the active power switch has been substituted with passive switches D_1-D_2-D_4. By utilizing equations (1) and (2), the voltage ratio is obtained by

$$M = \frac{V_{Co2}}{V_{in}} = M_{p-triple} M_o = \frac{3}{1-D} \times 2 = \frac{6}{1-D} \tag{10}$$

The development of the output section in the triple-EC-based boost converter has allowed for different configurations in both the output and boosting sections. This results in various combinations, as illustrated in Figure 13. Therefore, new types of dc-dc converter with high ratio voltage boosting capability can be constructed. This flexibility in configuration allows for the optimization of the converter's performance and the achievement of specific voltage ratio requirements.

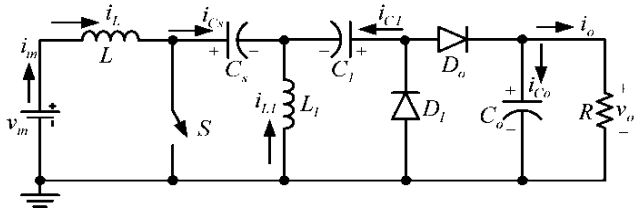

Figure 10. *Structure of the self-lift circuit.*

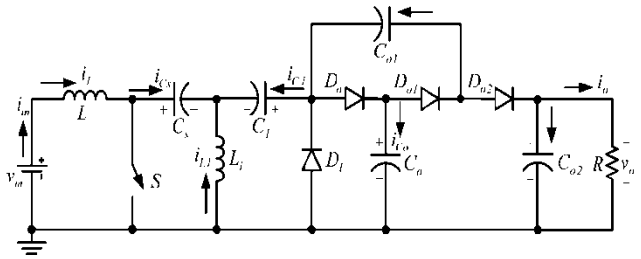

Figure 11. *The self-lift circuit of double-EC-based VL-type SEPIC converters.*

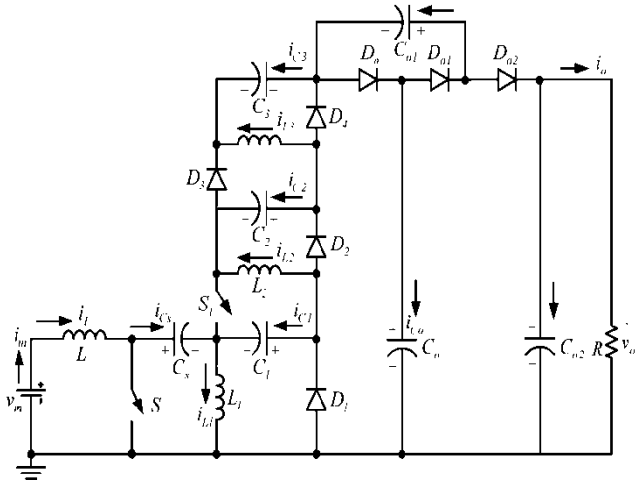

Figure 12. *Proposed triple-lift circuit of double EC based VL-type SEPIC converters.*

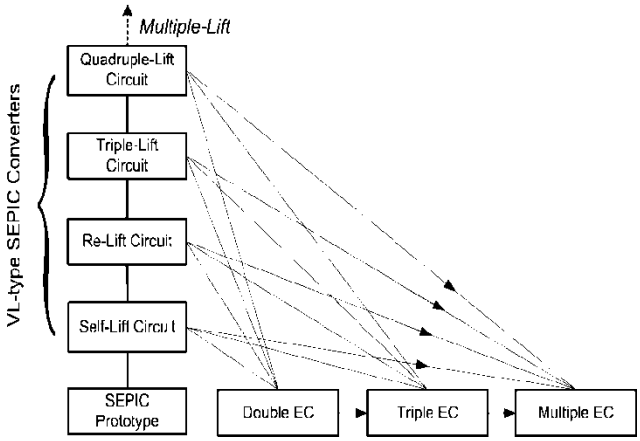

Figure 13. *Combination of VL-type SEPIC converters with output enhanced circuits.*

Under the assumption that the number of VL cells in the pump section is n_p and the number of VL cells in the output section is n_o, all the newly constructed topologies can be unified. Based on a previous analysis, a general formula for calculating the voltage ratio has been derived. The formula is as follows:

$$M = \frac{V_o}{V_{in}} = M_p M_o = \frac{[n_p + h(n_p) D^{h(n_p)}](n_o + 1)}{(1-D)} \tag{11}$$

Where: $h(n_2) = \begin{cases} 1 & n_p = 0 \\ 0 & n_p > 0 \end{cases}$

When $n_p = n_o = 0$, the unified topology degenerates to the prototype of the SEPIC converter as shown in Figure 13. Hence, from (11) we get

$$M = \frac{V_o}{V_{in}} = \frac{D}{1-D} = M_{SEPIC} \tag{12}$$

When n_o=0 and $n_p \geq 1$, we get

$$M = \frac{V_o}{V_{in}} = \frac{n_p}{(1-D)} = M_{main} \tag{13}$$

The other developed converters can be collectively referred to as enhanced series converters. As a result, the total number of components in these converters can be calculated as follows:

Numbers of active power switches: $\begin{cases} 1 & n_p = 0,1 \\ 2 & n_p > 1 \end{cases}$

Numbers of diodes: $2n_p + 2n_o - 1$

Numbers of inductors: n_p+1

Numbers of capacitors: n_p+2n_o+2

5. Simulation and Experimental Result

In verification of the theoretical calculations, the converters were simulated using the Psim simulation package. Testing circuits were created based on the typical topologies obtained from the design and theoretical calculations. The simulation results were then compared with the expected results determined from the calculations. This process was undertaken to ensure the accuracy and effectiveness of the converter designs and theoretical calculations.

5.1. The Triple-EC-Based Boost Converter

The corresponding topology is depicted in Figure 8. Given that $V_{in}=10V$, $R=100\Omega$, $L=500\,\mu H$, $C_{o1}=C_{o2}=22\,\mu F$, $C_o=47\,\mu F$ and $D=0.6$. All of the semiconductor switching devices are assumed to be ideal. The theoretical values are derived as follows:

$$V_o = MV_{in} = \frac{2}{1-D}V_{in}\Big|_{D=0.6} = 50V$$

$$V_{Co} = M_p V_{in} = \frac{1}{1-D}V_{in}\Big|_{D=0.6} = 25V$$

The results of the simulation can be seen in Figure 14, where curves 1-3 represent v_o, v_{Co} and v_{Cs},, respectively. The simulation accurately matches the theoretical analysis in terms of steady-state performance. In the hardware testing circuit, we have chosen to use the same parameters.

However, due to the influence of parasitic parameters, the practical output voltage is slightly lower than the theoretical values, which are demonstrated by the experimental curves during the steady-state in Figure 15. After conducting careful measurements, the output voltage V_o is displayed on Channel 1 (50V/Div), and the value of V_{Cs}, displayed on the same channel. Conclusions could be drawn that the measured results coincide with both of theoretical analysis and simulation outcomes.

5.2. The Triple-Lift Circuit of Double EC Based VL-Type SEPIC Converters

The topology that has been generated can be observed in Figure 12. Given that $V_{in}=10V$, $R=1k\Omega$, $L=L_1=L_2=L_3=500\,\mu H$, $C_s=110\,\mu F$, $C_1=C_{o1}=C_{o2}=22\,\mu F$, $C_o=47\,\mu F$, and $D=0.6$. The switching frequency is set to $100kHz$. In the same, all of the semiconductor switching devices are assumed to be ideal. The theoretical values are derived as follows

$$V_o = MV_{in} = \frac{6}{1-D}V_{in}\Big|_{D=0.6} = 150V$$

$$V_{Co} = M_p V_{in} = \frac{3}{1-D}V_{in}\Big|_{D=0.6} = 75V$$

The simulation results can be observed in Figure 16, with curve 1-3 representing v_o, v_{Co} and v_{Cs},, respectively. Performance of circuit in simulation matches the theoretical analysis in steady-state precisely.

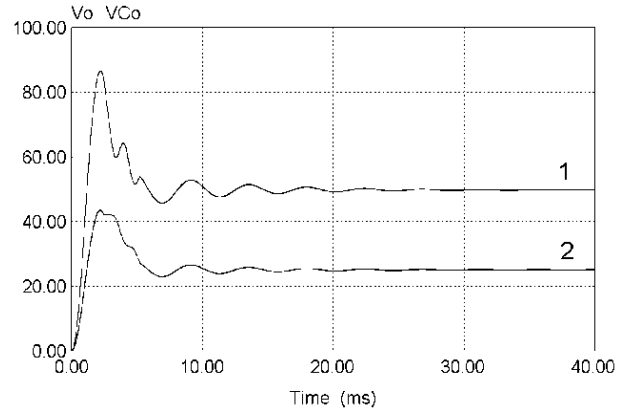

Figure 14. *Simulation results for the applied enhanced circuit.*

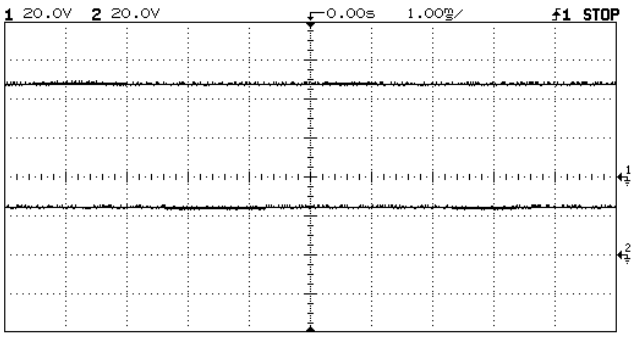

Figure 15. *Experimental results for the applied enhanced circuit.*

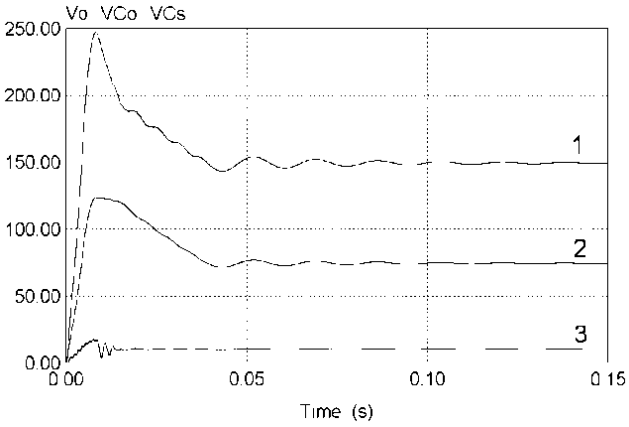

Figure 16. *Simulation results for the applied enhanced circuit.*

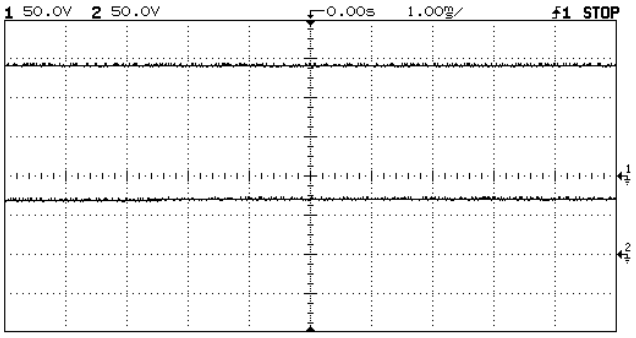

Figure 17. *Experimental results for the applied enhanced circuit.*

The corresponding experimental results during the steady-state are shown in Figure 17. After conducting careful measurements, the output voltage value of V_o, is displayed in Channel 1 (50V/Div), and the value of V_{Cs} are shown in the same channel. Conclusions could be drawn that the measured results coincide with both of the theoretical analysis and simulation outcomes.

6. Conclusions

This paper introduces the concept of development in the output section in order to achieve higher voltage-boosting capability. This concept enhances our understanding of the fundamental principles of power electronics. Several innovative output enhanced circuits are presented, which greatly improve the voltage boosting capability. Importantly, these new topologies do not require additional power switches or transformers, making them easily applicable in future industrial settings. The summarized guidelines for constructing these topologies are valuable for topology design and have educational benefits in the field of power electronics engineering.

Conflicts of Interest

The authors declare no conflicts of interest.

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